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10/715,064	11/17/2003	Anand Pande	15156US01	7036

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,064	PANDE, ANAND	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date. _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Remarks filed on November 9, 2006 regarding application 10,715,064 filed on November 17, 2003.

2. Claims 1-6 have been cancelled previously.

Claims 7-11 are pending for consideration.

3. ***Response to Remarks***

Applicants' amendments and remarks have been fully and carefully considered, with the Examiner's response set forth below.

Applicant contends that, in the invention of Kao et al. (US 6,263,410), the read pointer in figure 3 is implemented by a conventional sequential counter and the write pointer is implemented using a Gray code converter, while the read pointer in figure 3 is implemented by a Gray code converter and the write pointer is implemented using a conventional sequential counter, thus Kao et al. fails to teach a circuit with two Gray code counters.

However, in additional to the configurations illustrated in figures 3 and 9, Kao et al. also explicitly teach an embodiment, as shown in figure 2 and noted as **Prior Art**, where two Gray to sequential converters [In the design of FIG. 2, the asynchronous FIFO comprises two Gray code counters. One is used as a read pointer, and the other is used as a write pointer. To determine how much memory space in the FIFO memory can be accessed, the Gray codes corresponding to the read and write pointers are first converted to sequential counts. A subtraction is then performed on the two

sequential counts in order to determine the available space in the FIFO (column 1, lines 45-51)].

It is noted that the **Prior Art** shown in figure 2 alone teaches all the limitations recited in claim 1.

Therefore, the Examiner's position regarding the merits of patentability of all claims remains the same as stated in the previous Office Action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kao et al. (US 6,263,410).

As to claim 7, Kao et al. disclose **a circuit for storing data** [figures 1-9 show the details of the circuit], **said circuit comprising**:

a FIFO for queuing the data [dual port RAM FIFO, figure 3, 301; Apparatus and Method for Asynchronous Dual Port FIFO (title); An apparatus and method for controlling an asynchronous dual port FIFO memory is provided (abstract)];

a read pointer for indicating a particular address in the FIFO [Read Pointer, figure 9; in additional to the configurations illustrated in figures 3 and 9, Kao et al. also explicitly teach an embodiment, as shown in figure 2 and noted as **Prior Art**, where two Gray to sequential converters: In the design of FIG. 2, the asynchronous FIFO

comprises two Gray code counters. One is used as a read pointer, and the other is used as a write pointer. To determine how much memory space in the FIFO memory can be accessed, the Gray codes corresponding to the read and write pointers are first converted to sequential counts. A subtraction is then performed on the two sequential counts in order to determine the available space in the FIFO (column 1, lines 45-51); It is noted that the **Prior Art** shown in figure 2 alone teaches all the limitations recited in claim 1];

a write pointer for indicating another particular address in the FIFO [Write Pointer, figure 3, 304; in additional to the configurations illustrated in figures 3 and 9, Kao et al. also explicitly teach an embodiment, as shown in figure 2 and noted as **Prior Art**, where two Gray to sequential converters: In the design of FIG. 2, the asynchronous FIFO comprises two Gray code counters. One is used as a read pointer, and the other is used as a write pointer. To determine how much memory space in the FIFO memory can be accessed, the Gray codes corresponding to the read and write pointers are first converted to sequential counts. A subtraction is then performed on the two sequential counts in order to determine the available space in the FIFO (column 1, lines 45-51); It is noted that the **Prior Art** shown in figure 2 alone teaches all the limitations recited in claim 1];

a first Gray code to binary converter for generating the particular address indicated by the read pointer [figure 9 shows that the output of the Read Pointer is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2];

a second Gray code to binary converter for generating the particular address indicated by the write pointer [figure 3 shows that the output of the Write Pointer (304) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]; **and**

a comparator for determining whether the FIFO is empty or full based on a comparison of a Gray code associated with the read pointer and a Gray code associated with the write pointer [figures 3, 7 and 9; also see figure 2].

As to claim 8, Kao et al. teach that **a first Gray code generator for generating the Gray code associated with the read pointer** [figure 9 shows that the output of the Read Pointer (which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]]; **and**

a second Gray code generator for generating the Gray code associated with the write pointer [figure 3 shows that the output of the Write Pointer (304, which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]].

As to claim 9, Kao et al. teach that **a first Gray code to binary converter for generating the particular address indicated by the read pointer** [figure 9 shows that the output of the Read Pointer is fed to a Gray Code to Sequential Converter to

generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]]; **and**

a second Gray code to binary converter for generating the another particular address indicated by the write pointer [figure 3 shows that the output of the Write Pointer (304, which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]];

wherein the first Gray code to binary converter receives the Gray code associated with the read pointer from the first Gray code generator [figure 9 shows that the output of the Read Pointer is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]]; **and**

wherein the second Gray code to binary converter receives the Gray code associated with the write pointer from the second Gray code generator [figure 3 shows that the output of the Write Pointer (304, which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]].

As to claim 10, Kao et al. teach that **the FIFO comprises a FIFO RAM** [dual port RAM FIFO, figure 3, 301; Apparatus and Method for Asynchronous Dual Port FIFO (title); An apparatus and method for controlling an asynchronous dual port FIFO memory is provided (abstract); also see figure 2]].

As to claim 11, Kao et al. teach that **a method for storing data** [figures 1-9 show the details of the circuit], **said method comprising**:

queuing the data in a FIFO [dual port RAM FIFO, figure 3, 301; Apparatus and Method for Asynchronous Dual Port FIFO (title); An apparatus and method for controlling an asynchronous dual port FIFO memory is provided (abstract); also see figure 2]];

indicating a particular read address in the FIFO [figure 9 shows that the output of the Read Pointer is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]];

indicating a particular write address in the FIFO [figure 3 shows that the output of the Write Pointer (304, which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]]:

generating the particular read address by converting a first Gray code to binary [figure 9 shows that the output of the Read Pointer is fed to a Gray Code to Sequential Converter to generate the address to access the dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]];

generating the particular write address by converting a second Gray code to binary [figure 3 shows that the output of the Write Pointer (304, which is Gray coded) is fed to a Gray Code to Sequential Converter to generate the address to access the

dual port RAM FIFO; note that the sequential code in a binary code; also see figure 2]];

and

determining whether the FIFO is empty or full based on a comparison of the first Gray code associated and the second Gray code [figures 2, 3, 7 and 9].

6. ***Related Prior Art Of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Hsu et al., (US 6,845,414), "Apparatus and Method of Asynchronous FIFO Control."
- Camilleri et al., (US 6,434,642), "FIFO Memory System and Method with Improved Determination of Full and Empty Conditions and Amount of Data Stored."
- Shyi et al., (US 5,426,756), "Memory Controller and Method Determining Empty/Full Status of a FIFO Memory Using Gray Code Counters."
- Brooks et al., (US 5,410,664), "RAM Addressing Apparatus with Lower Power Consumption and Less Noise Generation."
- Cohn et al., (US 4,556,960), "Address Sequencer for Overwrite Avoidance."
- Jiang, (US Patent Application Publication 2004/0207547), "Method of Scalable Gray Coding."
- Pontius, (US 6,337,893), "Non-Power-Of-Two Gray-Code Counter System Having Binary Incrementer with Counts Distributed with Bilateral Symmetry."
- Yi, (US 6,703,950), "Gray Code Sequences."

Conclusion

7. Claims 7-11 are rejected as explained above.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

December 4, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
12/4/06